BUILT-IN SELF TEST SYSTEM AND METHOD FOR HIGH SPEED CLOCK AND DATA RECOVERY CIRCUIT

Abstract of the Disclosure

A built-in self test system for testing a clock and data recovery circuit is disclosed. The present invention provides a built-in self test circuit which operates with high speed phase lock loop. The built-in circuit comprises data generating means for generating a test data byte and serializing means coupled to the data generating means for converting the test data byte into serial test data. The clock and data recovery means are coupled to the output of the serializing means for recovering the clock and test data from the serial test data. A deserializing means coupled to the output of the clock and data recovery means converts the recovered serial test data into a recovered test data byte, and analyzing means connected to the output of the deserializing means compares the recovered test data byte to the initial test data byte.